FPL 2025

Adaptable Integrated Circuits for an Evolving World

BECAUSE THE ONLY CONSTANT IS CHANGE!

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FPL, Leiden, September 3, 2025

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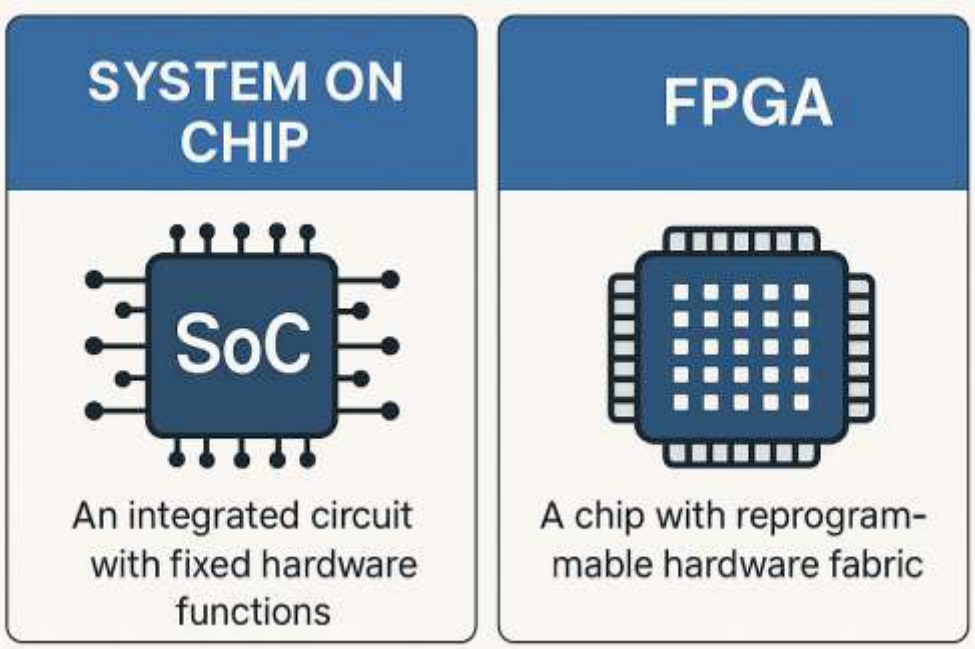
FPGAs are cool…. What about SoCs?

SoC vs FPGA according to … chatGPT



Feature	SoC	FPGA
Hardware Flexibility	Fixed (cannot change after tapeout)	Fully reprogrammable
Performance	Optimized, high performance	High for parallel tasks, lower clock speeds
Power Efficiency	Very high (optimized silicon)	Lower (due to programmable fabric)
Cost per Unit	Low at scale (mass production)	Higher (per chip)
Development Time	Long (requires ASIC design cycle)	Short (design, test and reprogram quickly
Best For	Consumer devices, mase products	Prototyping, specialized low-volume or evolving systems

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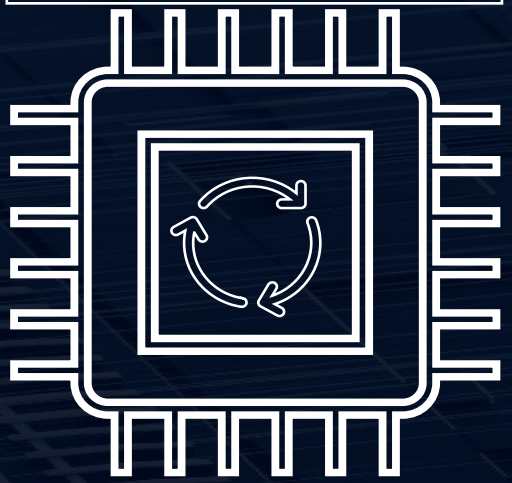
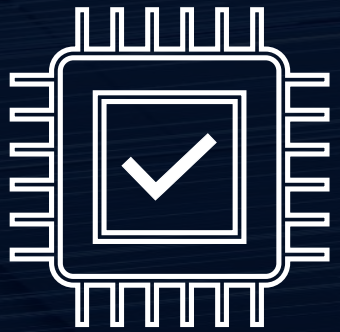
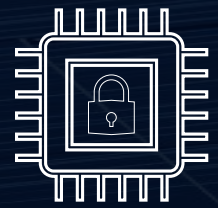
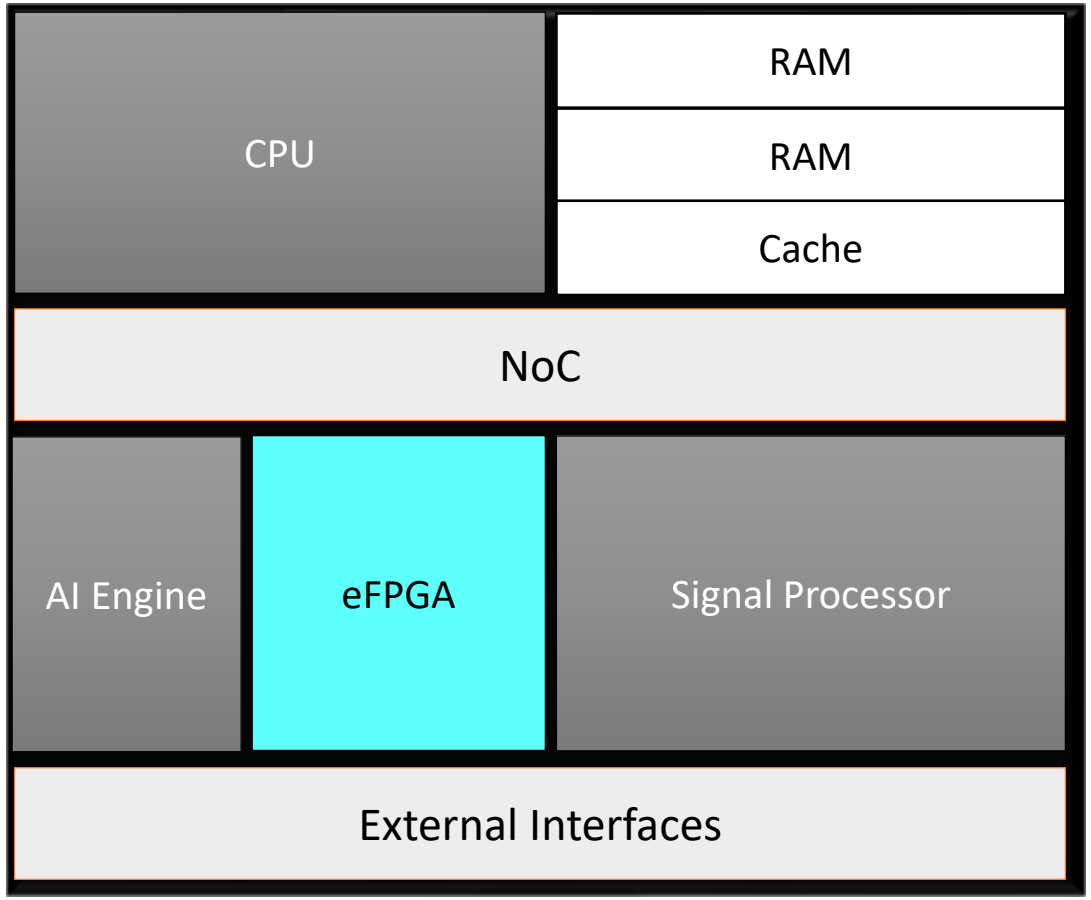
What if…

We could get Best of Both worlds

	FPGA	HYBRID	ASIC
			
PROS	Flexible, Adaptable	Adaptable Hardware High Performance Low Cost & Power Lowers Design Risk	Highest Performance Lowest Cost & Power
CONS	High Cost & Power Supply Chain Trust Cloneable/Mutable Side Channel Attacks Hard to Design	RTL design knowledge for highest performance	Lacks any HW adaptability or flexibility High Design Risk Only SW upgrades

Hybrid solution with an eFPGA



3 structural megatrends imply an exponential requirement for adaptive ICs

1 Growing demands for long lifetime ICs

2 End of Moore's law

Importance of custom compute

3 Enabling changes in a design

Better TTM, less verification and solving HR issues

New growing requirements

- Adaptation during chip lifetime
- Adaptive accelerators /**Custom** compute
- Lower design cycles with automation
- Pushing design decisions to after tapeout
- Waste reduction

Maximize SoC Value with Embedded eFPGA

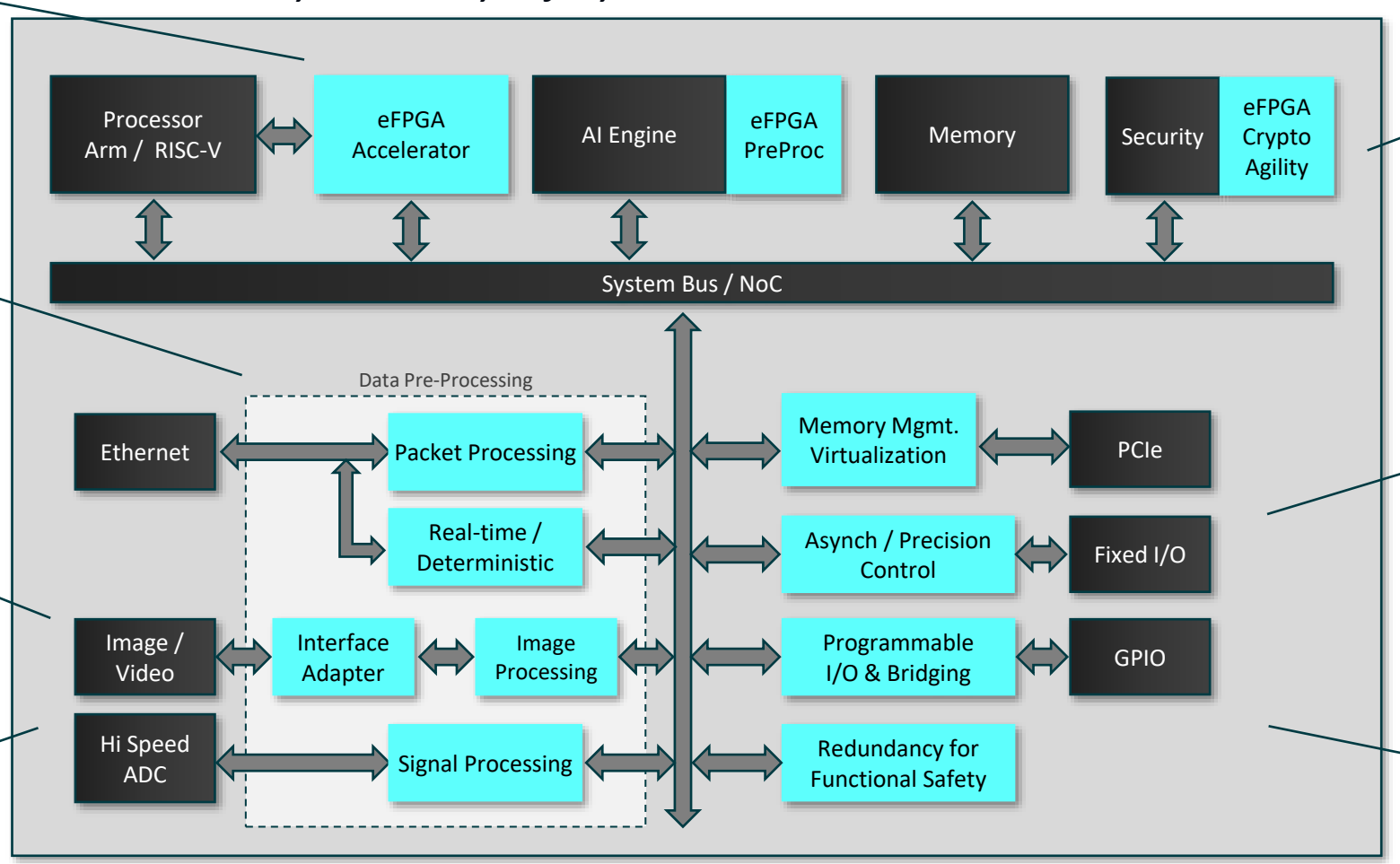
Security. Flexibility. Lifecycle Extension

Accelerate complex algorithms with custom ISA Instructions

Programmable Data Plane Processing Deterministic Industrial Networking

Adaptable Image Signal processing adapts to more sensors, increasing SAM

DSP Filtering Transforms



Protect against evolving threats & quantum computing

Obfuscate secret IP

Enable security autonomy

Expand Physical and Virtual functions Bridge & DMA data

Interface Flexibility – Adaptable to different markets & applications

Eliminate unused ports – minimizing surface attack exposure

Menta eFPGA IP

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Cross-Industry Benefits of eFPGA IP

Flexible by design, eFPGA delivers domain-specific advantages in every sector — from aerospace to IoT

		A&D	Comms	FinTech	Auto	Industrial	Medical	Consumer / Edge IoT
Security	Crypto Agility, Obfuscation, Side Channel Attack Mitigation, Autonomy	✓	✓	✓	✓	✓	✓	✓
AI Adaptability	Adopt Novel Algorithms, Support Quantized NNs, Optimize & Reduce Memory	✓	✓	✓	✓	✓	✓	✓
Algorithm Acceleration	Algorithm Adapt & Accel, Power & Memory Efficiency, Determinism	✓	✓	✓	✓	✓	✓	✓
Signal Processing	Configurable DSP,FIR+IIR, Tightly Coupled Memory, Real-time Processing	✓	✓	✓	✓	✓	✓	✓
Interface Flexibility	Protocol Bridging, Dynamic Memory Mapping, Time Domain Synchronization	✓	✓	✓	✓	✓	✓	✓
Design Insurance	Risk Reduction, Debug, SKU Consolidation & Compliance Support	✓	✓	✓	✓	✓	✓	✓

PIONEERS OF EFPGA IP

15+YEARS

of Proven Innovation

ANY FOUNDRY
ANY NODE
100%
3rd-party Standard Cell

Global footprint with HQ

FRANCE

presence 10+ countries

ADVANCED ARCHITECTURE **ADAPTABLE**

LUT6
Adaptive DSP
3rd-Party Memory
Any Hard Macro Integration

IP DELIVERY

< 2 WEEKS

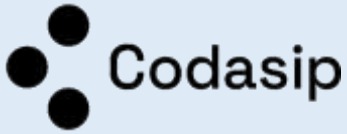
TRUSTED BY **LEADING CUSTOMERS** WORLDWIDE

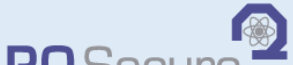
AI, Security/Crypto, RF Digital Front End, FSMs, Bridging
5G, Aerospace, Consumer, Defense, IIoT, Mobility, ICT Security

Customers and Partners

Customers

Menta Acceleration Partners





Value of Adaptable Hardware in ASIC & SoCs

Save Money

De-risk designs by moving risky IP to adaptable hardware

Hardware Flexibility

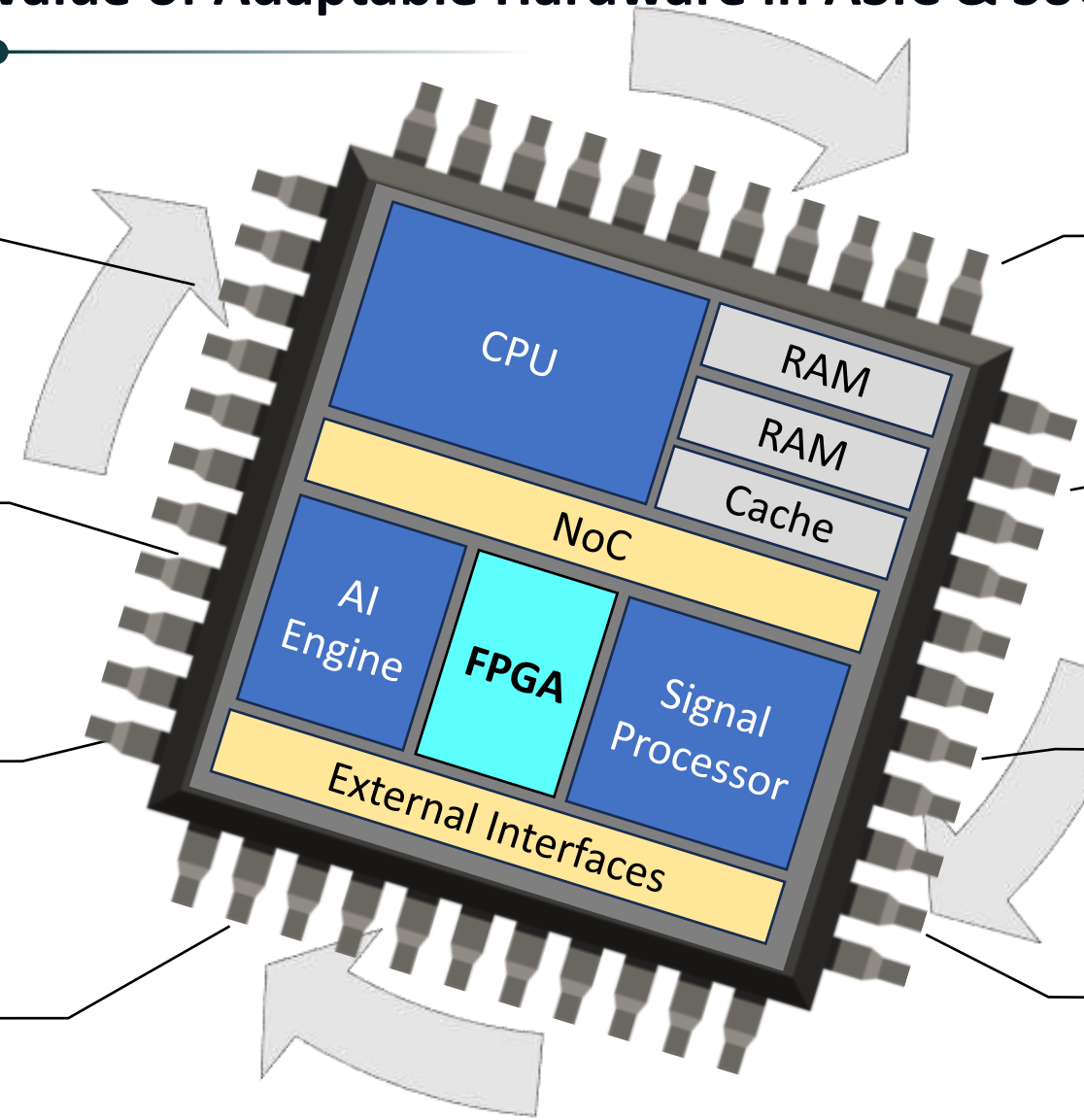
Extend product life by adapting to new algorithms & protocols such as AI and cryptography

Higher Performance

Faster due to direct internal connections and advanced nodes. Very low latency

Periodic Bug Fixes

Resolve bugs & improve IP efficiency



Regional Requirements

Meet regional specific protocol and security requirements in one IC

Lasting Security

Enable crypto agility to adopt novel cryptography algorithms as well as enable obfuscation & autonomy

Lifecycle Test & Debug

Built in Logic Analyzer w/ run-time debug, bring up analysis
Enable RMA Analysis

Enable Differentiation

Flexibility and adaptability to enable unique features vs competition

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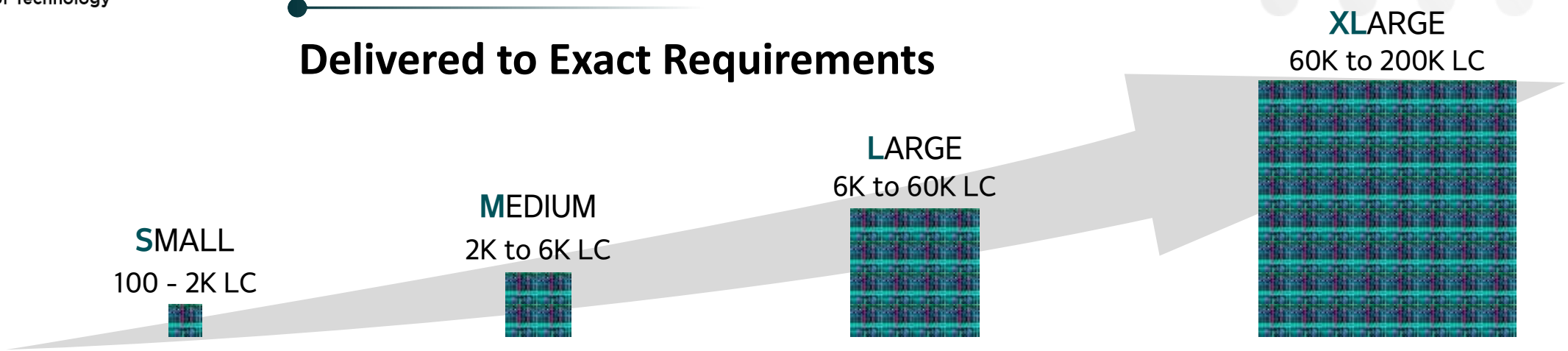
Scalable eFPGA IP

Delivered to Exact Requirements



eFPGA IPs examples available in Origami Programmer								Custom
	Small		Medium	Large		XLArge		Your IP
Feature	M5S0.5	M5S2	M5M5	M5L15	M5L40	M5XL65	M5XL130	?
# LC	596	1 605	4 815	14 884	40 128	65 664	130 000	?
# Adaptive DSP	0	6	11	24	60	25	1000	?
# Specific arithmetic block	-	-	-	-	-	-	-	?
SRAM (kb)	0	0	1 442	0	1 966	2 425	5 252	?
# IOs	667	844	1 388	3 436	3 808	4 770	6 500	?

100% Flexibility – Meet your exact specifications

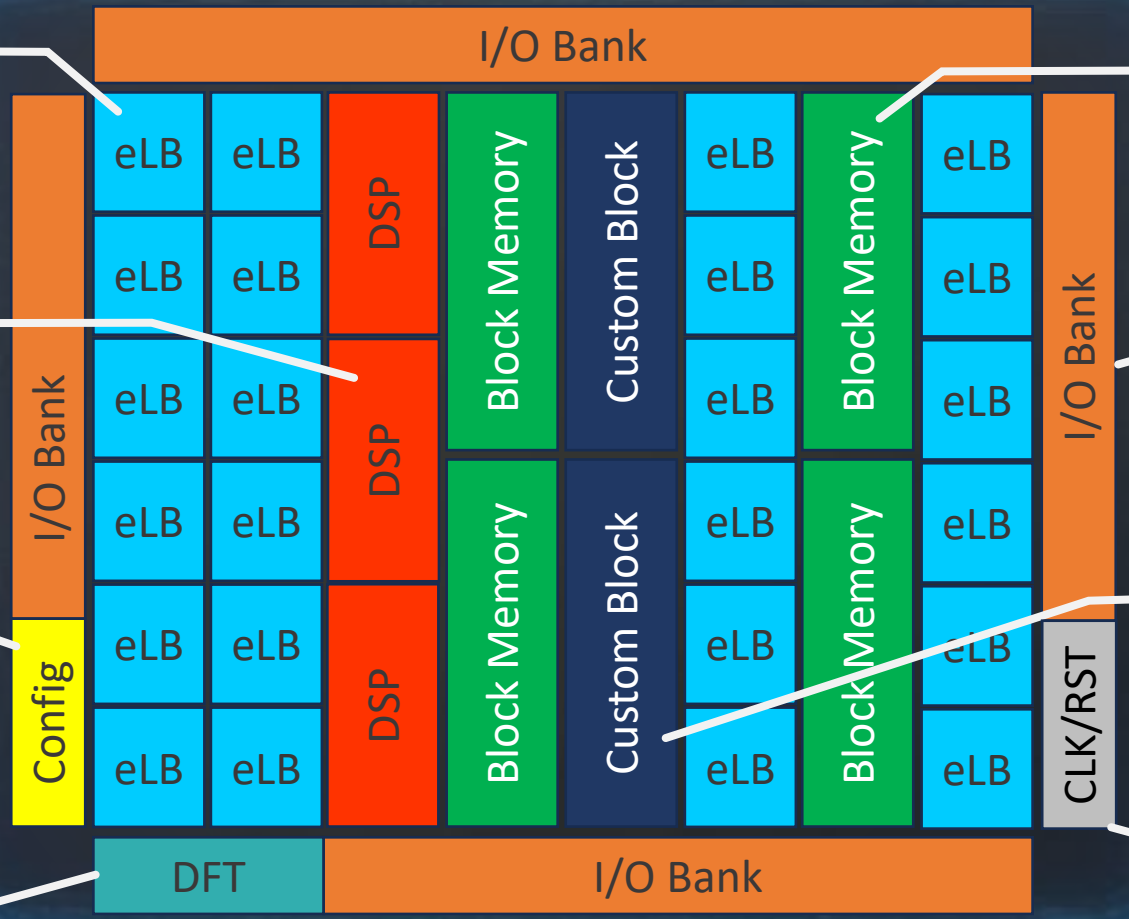
5th Generation DESIGN ADAPTIVE eFPGA IP

Embedded Logic Blocks
Menta 6-input LUT

DSP Blocks
Customer Defined

Configuration
SPI | AXI | JTAG
AHB | Custom

DFT
Standard ASIC test scan chain interface



Embedded Memory Blocks
Any 3rd-party RAM

I/O Pins
Define # of pins

Embedded Custom Block
Customer or 3rd-party IP

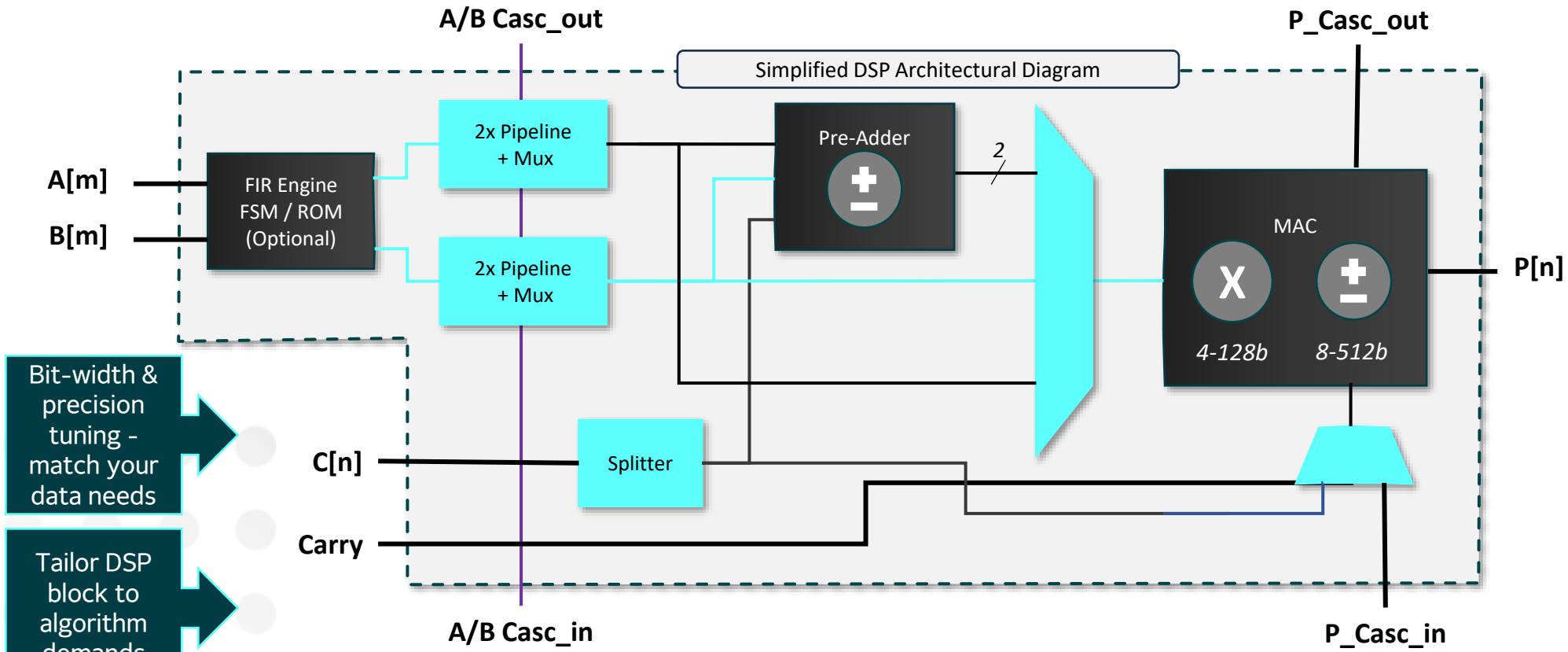
Clock / Reset
Control Input Block

100% Adaptable DSP Architecture

DSP configuration optimized by Origami based on the RTL design

4 to 512 Taps ROM for Coef's | Input Register Pipeline (0,1,2) | Pre-Adder Stage: Dynamic Input | Multiplier Stage: Products for 4 inputs | Arithmetic Stage: Cascadable for larger fxns

All Stages Optionally Registered with Shared CLK/RESET



Bit-width & precision tuning - match your data needs

Tailor DSP block to algorithm demands

DSP Examples

- Convolution
- Filtering
- Modulation and demodulation
- Mixing/summing/ decimation
- Image processing (Kernel Mathematics)
- Matrix Mathematics (Capable of Real and Complex numbers)
- FFT, DFT
- Correlation, etc.
- Software Defined Radio - I/Q schemes

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Any Foundry Support

100% 3RD PARTY STANDARD CELLS BASED

Support of any CMOS foundry, technology node, metal stack and process option

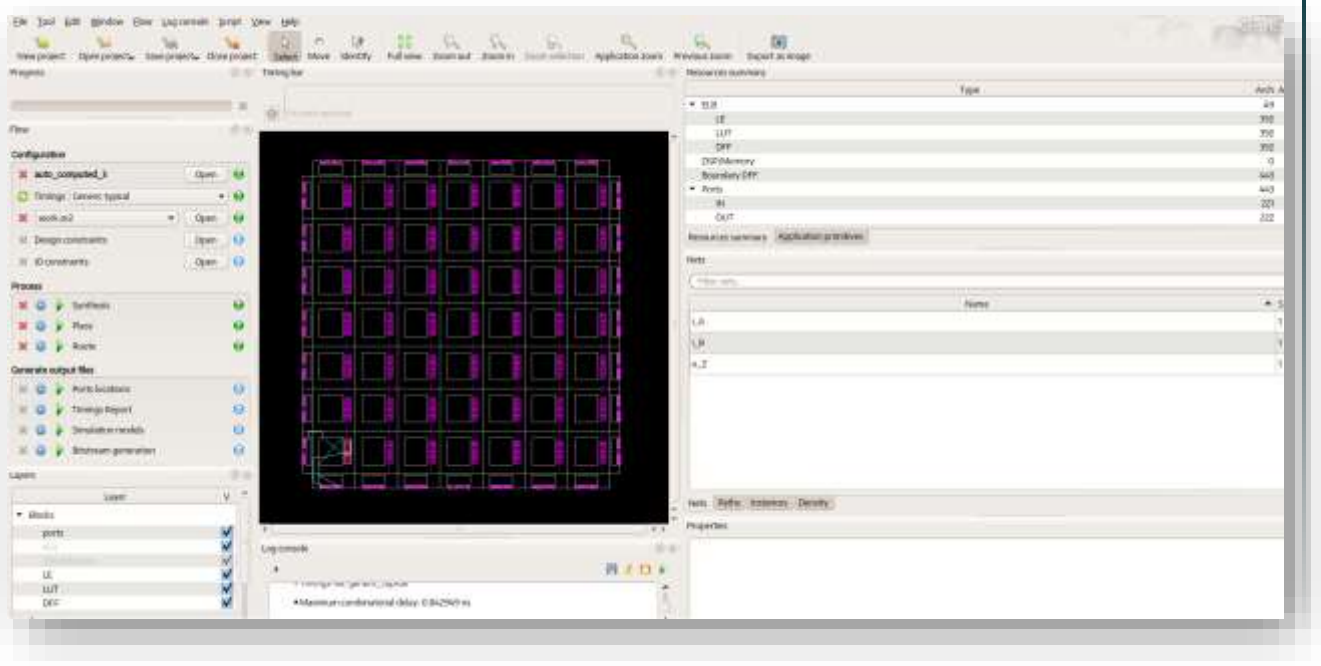
Tapeouts done or in progress

GlobalFoundries	intel foundry	skywater	ST life.augmented	TSMC	xfab
32 SOI	16	RH90	130	0.18um	XH 018
22 FDX	18A		65 LP	40 uLP	
12 LP / LP+			28 FD SOI	28 HPC+	
				12 FFC	
				N7	

Origami Programmer

FROM RTL TO BITSTREAM GENERATION

- **Inputs:**
  - Application RTL
    - IEEE Verilog / SystemVerilog / VHDL
  - Constraints: timing & IOs
- **Outputs:**
  - Bitstream
  - Simulation model
  - Timing reports
- **GUI interface:**
  - STA
  - Resources visualisation
  - Congestion maps
  - Move and reallocate resources
- **From synthesis to bitstream generation: Menta development**
- **No external tool required**
- **Full Command Line/Scriptable**
- **Redistributable**



eFPGAs Delivered to Customer Specifications

Soft IP

RTL for hardening by the customer with 100% Flexibility

- IP Specifications with Menta support
- eFPGA IP RTL delivered in **weeks** with EDA Support
- Physical design with the customer EDA environment

Hard IP

GDSII for customer's selected technology

- IP Specifications with Menta support
- Physical implementation Statement of Work
- GDSII and Timing Files delivered for integration

Crypto Agility

Problem statement:

- Security market geographical fragmentation
- Qualification problems: security algorithms used for export control

Case Study:

Chip designed in the USA, then sent to China to be assembled in a system sold in Europe

How to avoid sharing export-controlled security elements?

2 solutions

1

Crypto in SW. requires massive chip & computing capability

—

Only doable for large chips

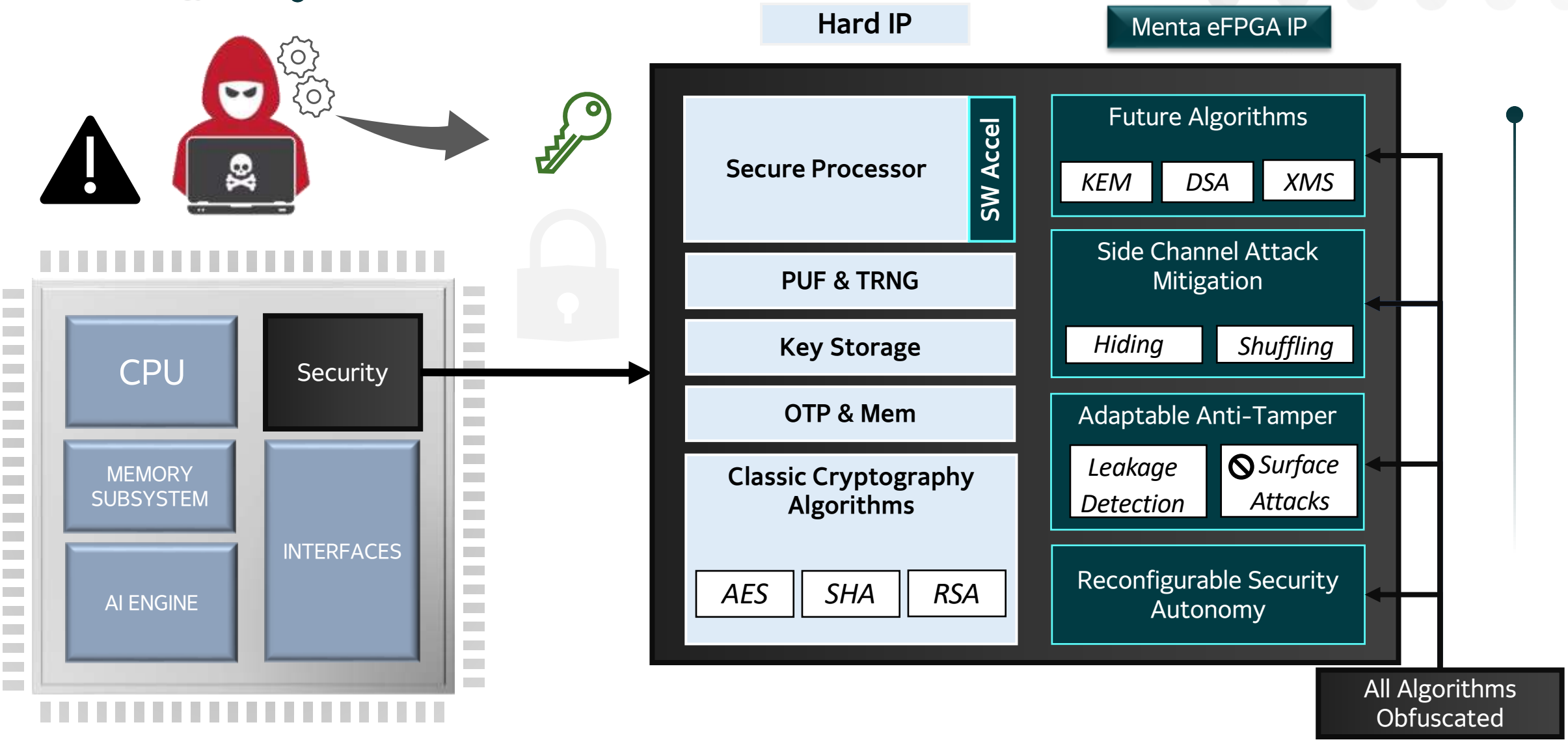
2

Crypto in reconfigurable logic: eFPGA

Most effective solution

eFPGA IP

Agile Cryptography Controller Architecture



Unique IP Identifier – Watermark & Blockchain

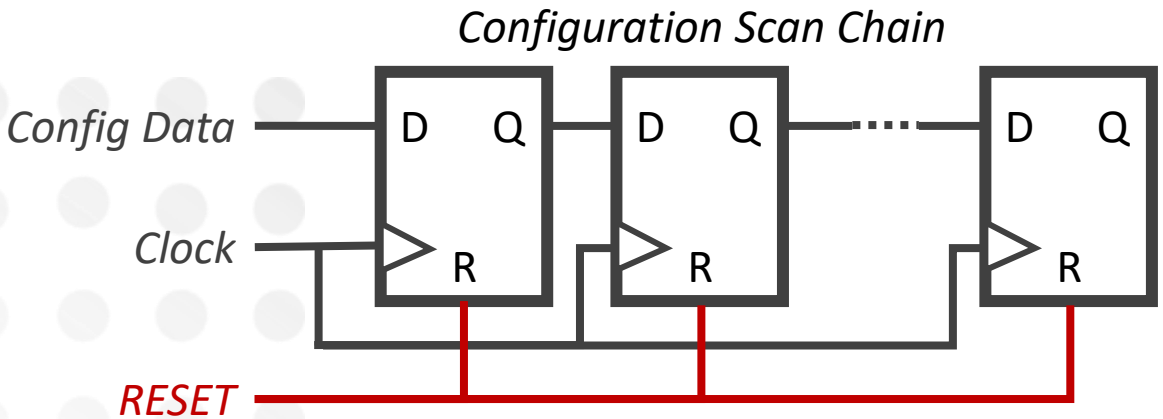
Each Menta eFPGA IP is **specifically** tailored to individual customer implementations

- Securely tracked using a unique watermark, blockchain ID and certificate
- Ensures complete isolation between customer implementations
- Superior security by generating a distinct bitstream for every IP instance
  - Virtually impossible for unauthorized parties to reverse-engineer or compromise the FPGA design

Instantaneous Hacking Mitigation

Resettable Configuration DFF

- eFPGA DFFs can be **erased** one clock cycle!
- Highly valuable in security applications for triggering events such as intrusion detection



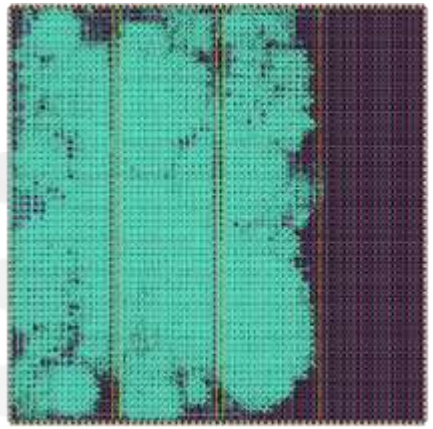
Full Response Control

- Wipe device, obfuscating the entire eFPGA design
- Optionally, disable interfaces or entire ASIC or SoC
- Protect data and firmware from malicious intentions

PQC Algorithms Implementations on Menta eFPGA IP

PQSecure-CRYSTALS-1000:

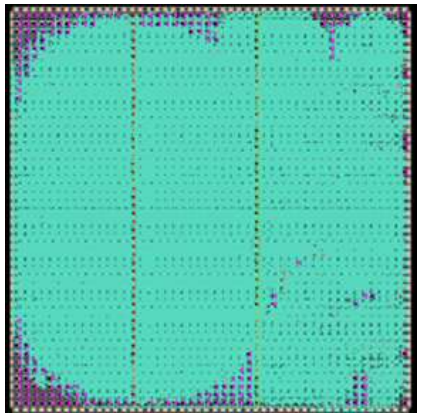
A unified hardware IP for CRYSTALS-KYBER and CRYSTALS-Dilithium with protection against Simple Power Analysis (SPA) and First-Order Differential Power Analysis (DPA) attack protection achieved through masking and shuffling. Timing attack protection through constant-time operation



Fmax*	LUTs	Flops	DSP	Memory
64	13,814	5,344	3	36

xQlave® ML-KEM (XIP6110B)

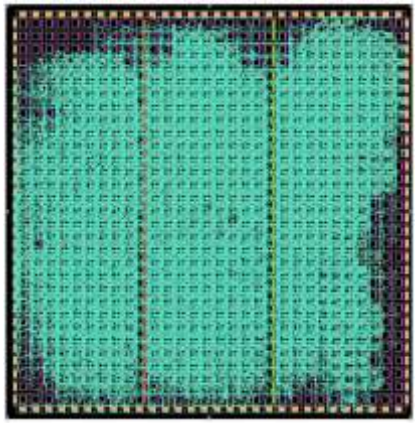
Kyber Key Encapsulation Mechanism IP core provides quantum-resistant key exchange, offering a secure solution against the growing threat posed by quantum computing.



Resources usage: <10K LUTs
Resources utilization: > 91%
Frequency*: 112 MHz

KiviPQC-KEM

Key Encapsulation that supports key generation, encapsulation, and decapsulation operations for all ML-KEM variants standardized by NIST in FIPS 203. ML-KEM is a post-quantum cryptographic (PQC) algorithm, designed to be robust against a quantum computer attack.



Fmax*	LUTs	Flops	DSP	Memory
84	6720	6720	25	10

* TSMC 28HPC+

Strong Security Partner Ecosystem

Menta Acceleration Security Partners provide solutions & expertise for long-lasting ASIC security

Software Acceleration with Custom ISA Extensions

HW/SW Co-Design tightly couples adaptable & reprogrammable hardware to the processor and provides the following benefits

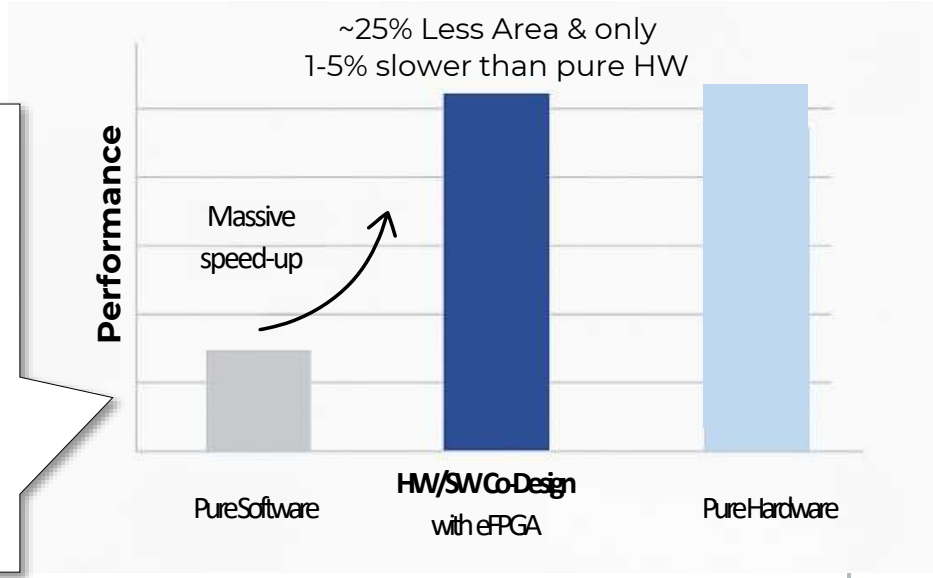
Increased Performance

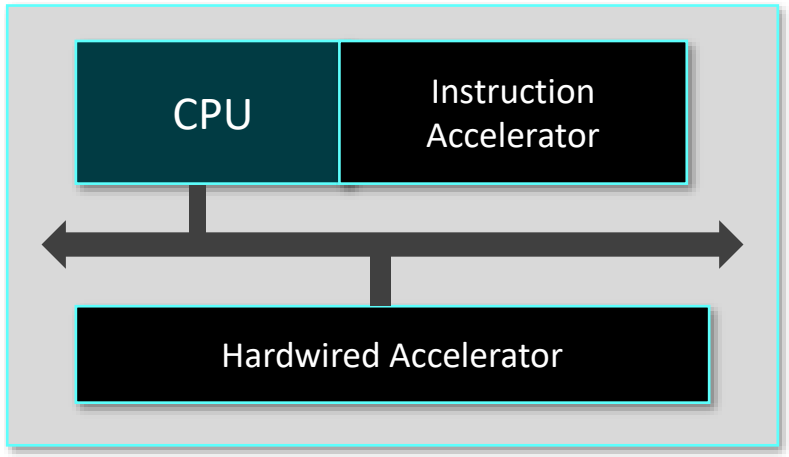
Lowers Latency

Reduces Power

PQC Algorithm with Hash function accelerated in FPGA

Other popular fxn's:
- Vector Math
- Floating Point
- Convolutions
- MAC Accel.
- DGEM
- Filters





Two Implementation Strategies

1. Tightly coupled to CPU for custom instruction extensions
   - Balance of performance and IP area impact
2. NoC connected accelerator
   - Highest performance & flexibility

Many Processors support Custom Instruction Extensions

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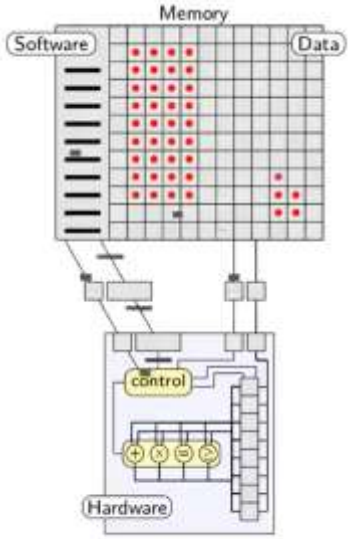
Where Do I Execute My Algorithm?

Processors or microchips offer ease-of-use, but in industries like Space, Communications, FinTech and others, need high performance, flexibility, and reliability – making FPGAs the obvious choice

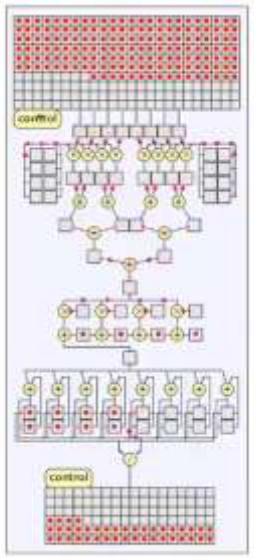
Common User Interfaces

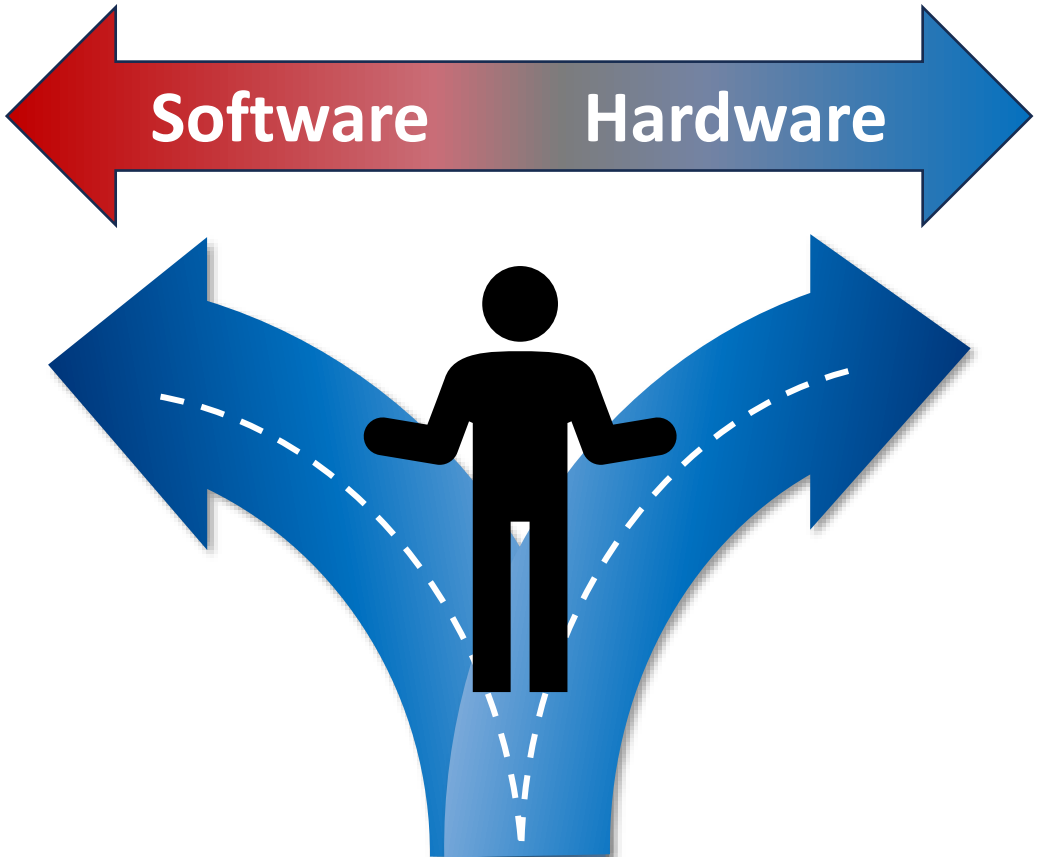
Non-time-sensitive task

Complex state machines with many branches



Normal processor

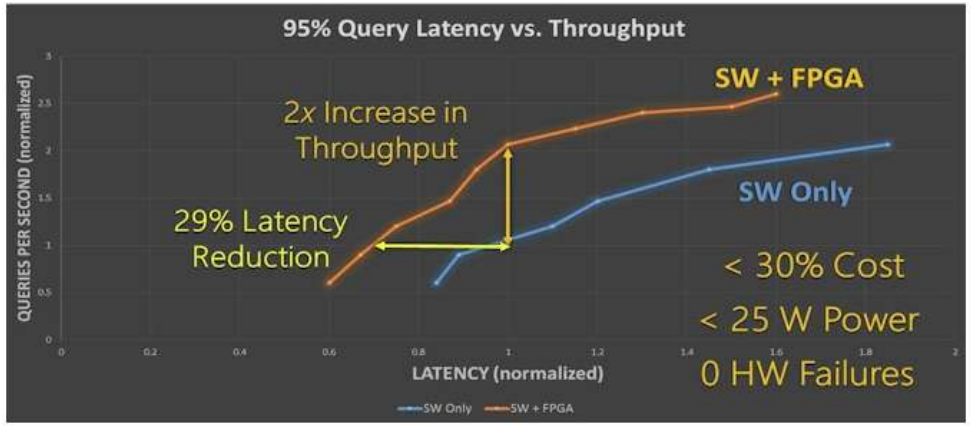

FPGA

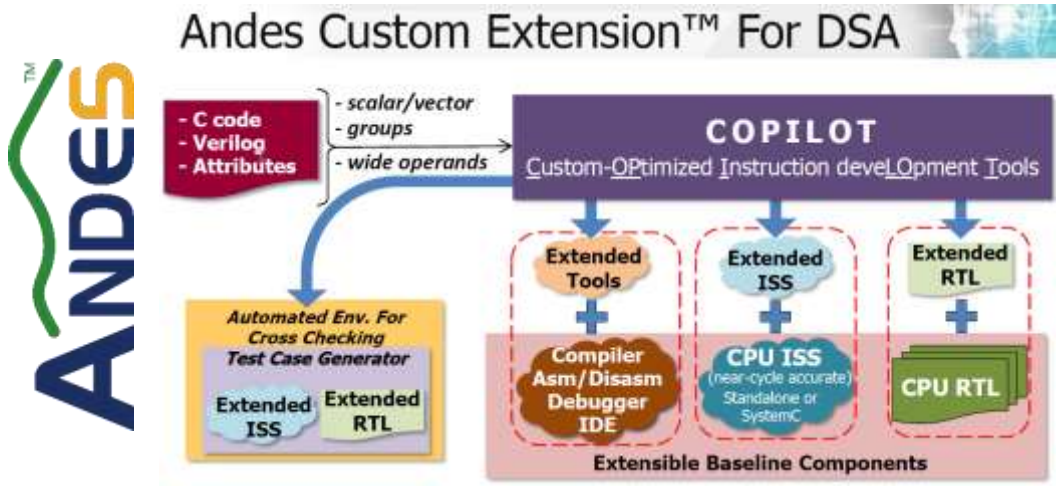


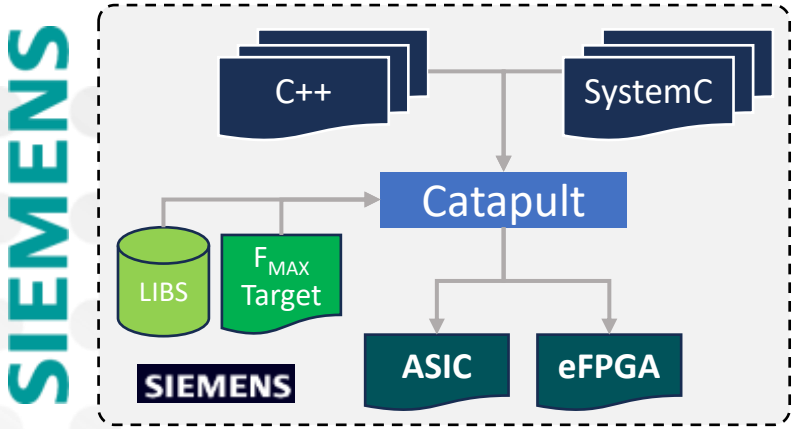
1. **High-Speed, Low Latency**
   HW Built to match exact needs of the application
2. **Parallel Processing**
   Simultaneous processing of multiple tasks & instructions
3. **Deterministic Processing**
   No cache latency & tightly coupled memory, pipelining
4. **Energy Efficiency**
   Optimized execution in HW reduces power consumption
5. **Enhanced Security**
   Safer key storage & threat mitigation, obfuscation

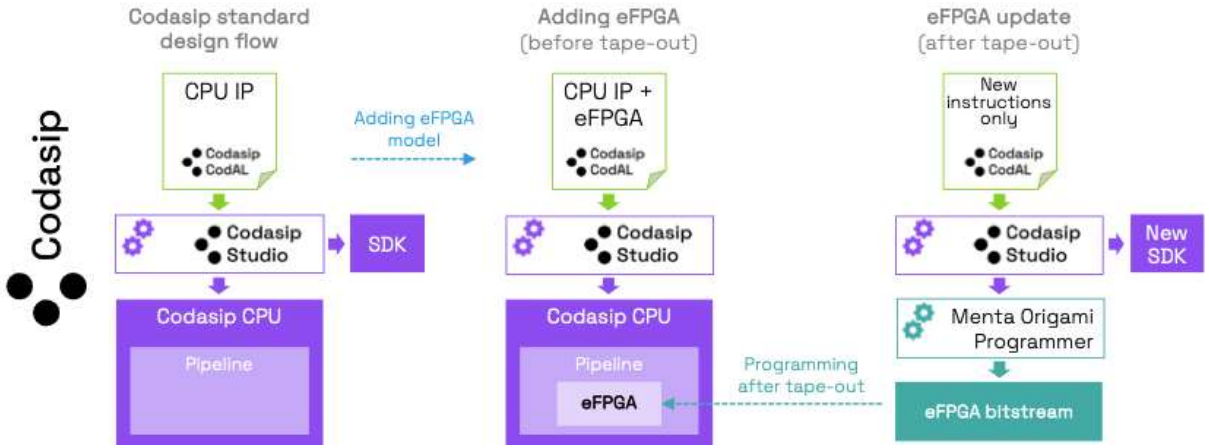
Proven HW/SW CoDesign Tools with Menta eFPGA IP

1,632 Servers with FPGAs Running Bing Page Ranking Service (~30,000 lines of C++)









Enables Post Silicon Reconfigurability

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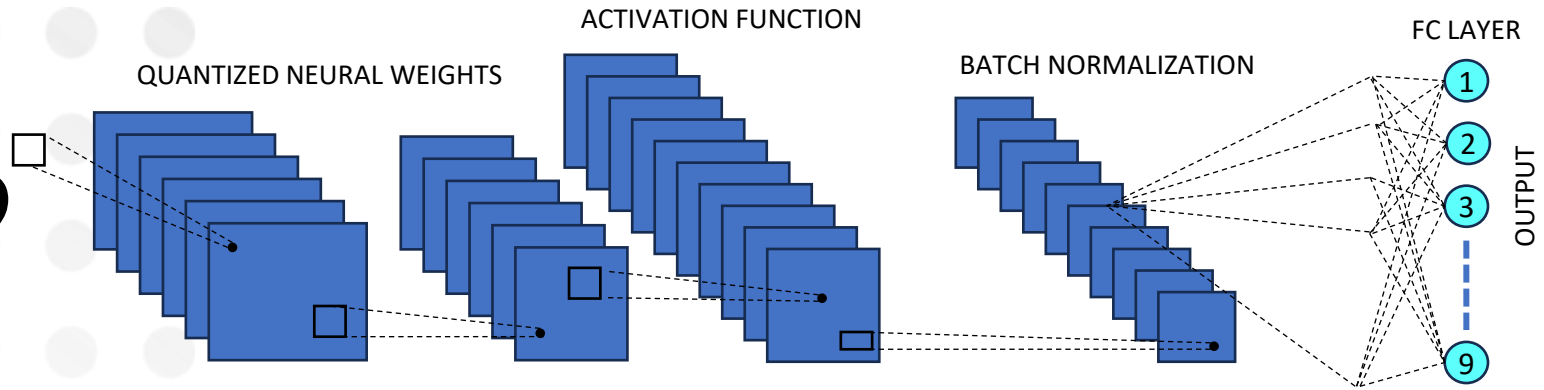
Highly Efficient AI Implementation in FPGAs with QNNs

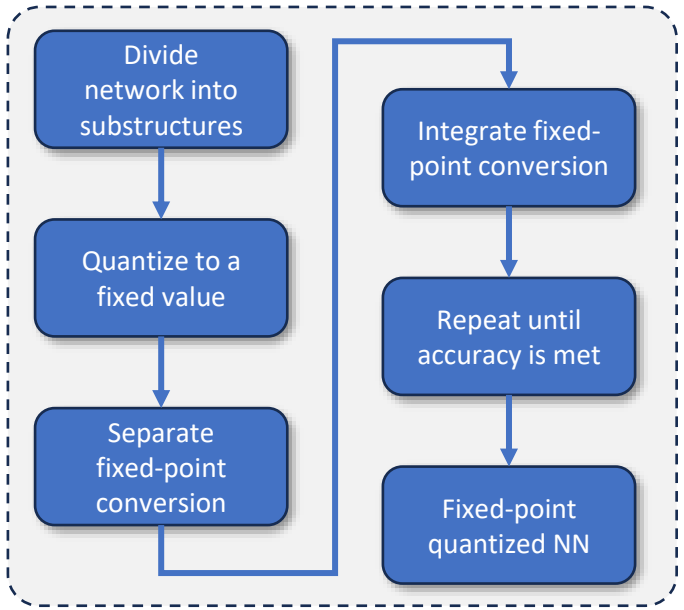
- Efficient AI algorithm execution is a function of two things:
  1. Processing architectures that exactly match the algorithm
  2. Effective software tool implementation into said architecture
- FPGA's flexible architectures can adapt to any network
- Quantized Neural Networks are rapidly gaining popularity
  - QNNs map very efficiently to FPGAs
    - Ultra low-latency with high performance
    - Very low memory footprint
  - New dataflow compilers are available for implementing QNNs on logic gate networks

Architectural Tradeoffs

Hardware	Cost	Flexibility	Performance	Power
CPU	Low	High	Low	High
GPU	High	Medium	High	Very High
ASIC	Very Low	Very Low	Very High	Very Low
FPGA	High	Medium	High	Low
eFPGA	Low	High	High	Low



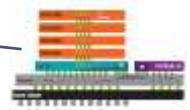
Quantized Neural Network



Optimize AI Memory Efficiency with eFPGA

Prevent AI Hardware Obsolescence with eFPGA Adaptability and Memory-Saving Techniques

Memory drives AI solution cost



DRAM
HBM

Large LLM & GenAI models are dominated by weights → memory

Save memory with
- Lossless LLM weight compression
- Structured sparsity
- New numerical formats

Compressed Weights

Weight Decompression

2x

Structured Sparsity Weight Population

2x

INT2/4 → INT8 Weight Remapping

4x

INT8/16 Weight Interface

TPU
AI Engine

Activation Functions & New Operators

Menta eFPGA IP

Adapt to changing AI Algorithms
Memory shim maximizes memory efficiency between models with different weights

- Different models & layers can employ different decompression & remapping techniques
- Deterministic latency with no loss of throughput

Output Activation & new operators in **existing HW**

eFPGA for AI: NimbleAI project

NimbleAI: Towards Next-generation Integrated Sensing-Processing Neuromorphic Endpoint Devices

DATE 2023

The NimbleAI sensing-processing architecture is to be specialized after-deployment by tunning system-level trade-offs for each particular algorithm in a given context. The target objectives of the NimbleAI: (1) 100x performance per mW gains compared to state-of-the-practice solutions (i.e., CPU/GPUs processing frame-based video); (2) 50x processing latency reduction compared to CPU/GPUs; (3) energy consumption in the order of tens of mWs; and (4) silicon area of approx. 50 mm^2.

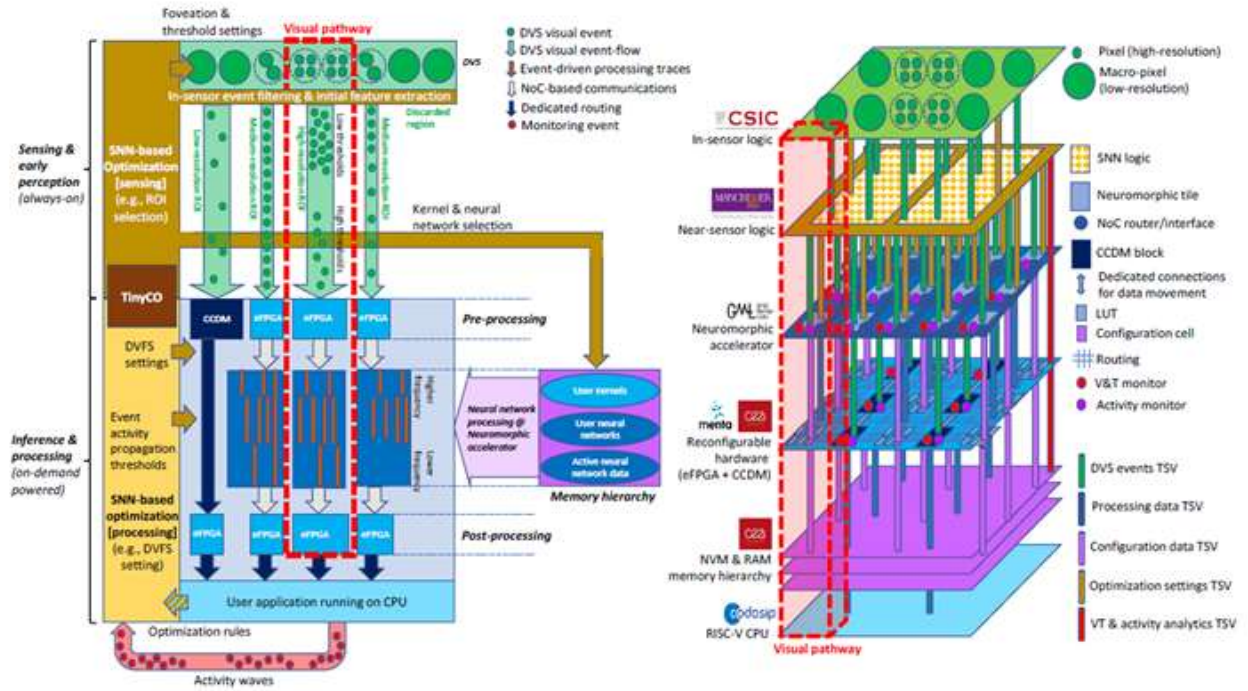
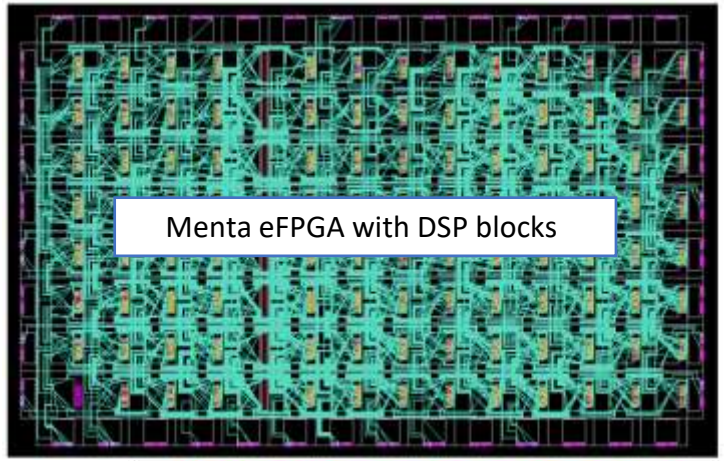


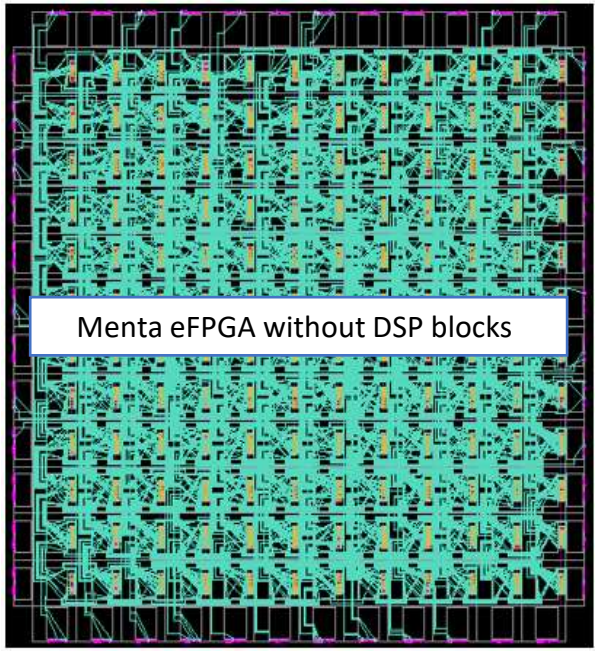
Fig. 2: NimbleAI: conceptual functioning (left) and 3D stacked conceptual architecture (right).

Implementation results: Systolic based convolution engine on Menta eFPGA

DSP impact in convolution implementation

Menta eFPGA resources	No DSP	With DSP
LUT	892	445
LE	1093	750
DFF	353	313
DSP	0	4
Fmax - Typical (MHz)	100.278	171.258
Fmax - Best (MHz)	185.34	331.185
Area (mm^2)	1.5112	1.1240
Power (mW)	0.7413	0.6731
eFPGA size	12x12	14x8





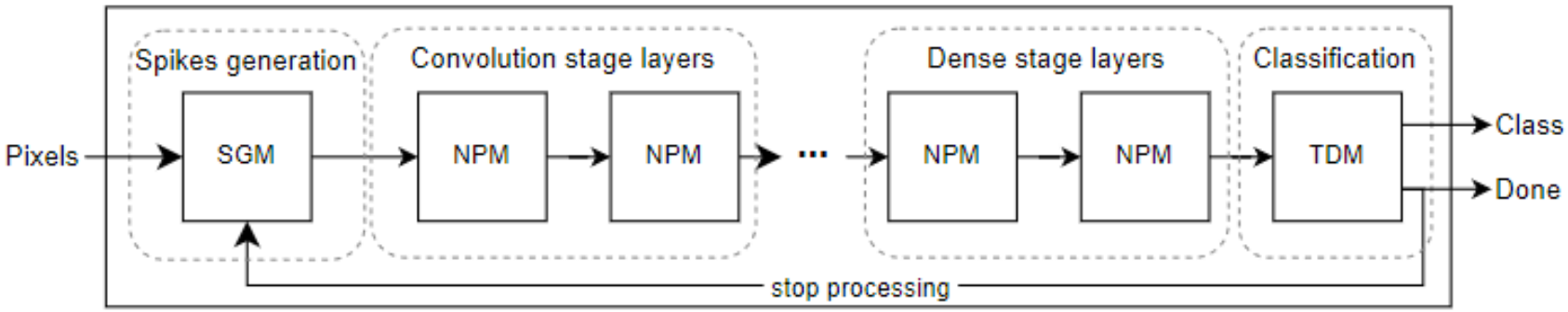
Menta eFPGA vs standalone FPGA and MCU (*)

Performance	Menta eFPGA	AMD Xilinx FPGA	Altera cyclone V	STM32 MCU
Frequency (MHz)	185	95	33	480
Execution time (ns)	400	357	508	5267 *10^6

(*) AMD : XC7A35TFTG256-1 | Altera : (5CEFA5M13C8) |
ST : STM32H743ZIT6U - Cortex-M7 | Menta: No DSP

Menta eFPGA for Spiking Neural Networks

- SPLEAT [1] : a generic hardware accelerator for Spiking Neural Network
  - Supports various spiking CNN definitions (configurable from ONNX, HdF5 or TFLite file formats)
- Developed by LEAT, an electronics laboratory of Côte d'Azur University
- Implemented application : Keyword Spotting on Google Speech Commands
  - CNN size : Input: 24x1x10 - Conv layers : 48 "3x1" – 48 "3x1" – 96 "3x1" – 35 "1x1"
  - Leaning framework is "SpikingJelly": SNN's open-source learning framework based on PyTorch.



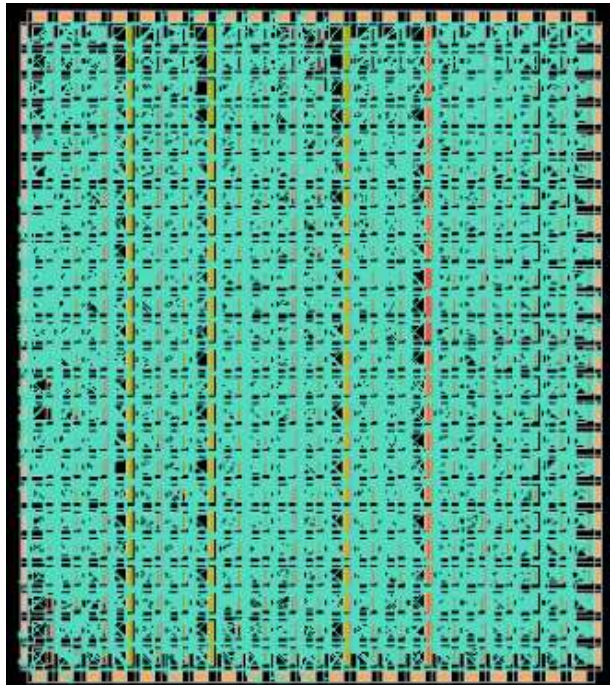
Reference: [1] N. Abderrahmane et al., "SPLEAT: SPiking Low-power Event-based ArchiTecture for in-orbit processing of satellite imagery," 2022 International Joint Conference on Neural Networks.

Implementation results: 21x24 eFPGA with 16x32 DSP blocks (with FIR engine)

Resources occupation by SPLEAT

Type	Arch	App	%
ELB	408	408	100.0%
LE	3264	3138	96.1%
LUT	3264	3026	92.7%
DFF	3264	1768	54.2%
DSP/Memory	44	38	86.4%
MNT_DSP_I16_32F32P	8	7	87.5%
MNT_Mem_2P2Kx16RFWE0_01E	36	31	86.1%
Boundary DFF	1420	0	-
Ports	1420	223	15.7%
IN	708	43	6.1%
OUT	712	180	25.3%
CLOCK	12	2	16.7%
IN	4	1	25.0%
OUT	4	0	-
INTERNAL	4	1	25.0%
SET/RESET	12	6	50.0%
IN	4	2	50.0%
OUT	4	0	-
INTERNAL	4	4	100.0%

SPLEAT mapping on 21x24 eFPGA with DSPs



Timing performance

- Clock name: i_slave_axis_aclk
- Max datapath delay: **302.317 MHz** (Minimum period between two sequential elements: 3.30778 ns)
- Longest path details:
  - Name: Longest path 1
  - Total delay: 3.30778 ns (100%)
  - Routing delay: 2.35125 ns (71.08%)
  - Logic delay: 0.956527 ns (28.91%)
  - Logic stages crossed: 12
- Maximum combinatorial delay: 0.414148 ns
- Maximum input to sequential element delay: 1.18927 ns (**840.852 MHz**)
- Maximum sequential element to output delay: 1.88203 ns (**531.340 MHz**)

Industrial Applications Requiring Adaptable Hardware

Industrial Automation & Control

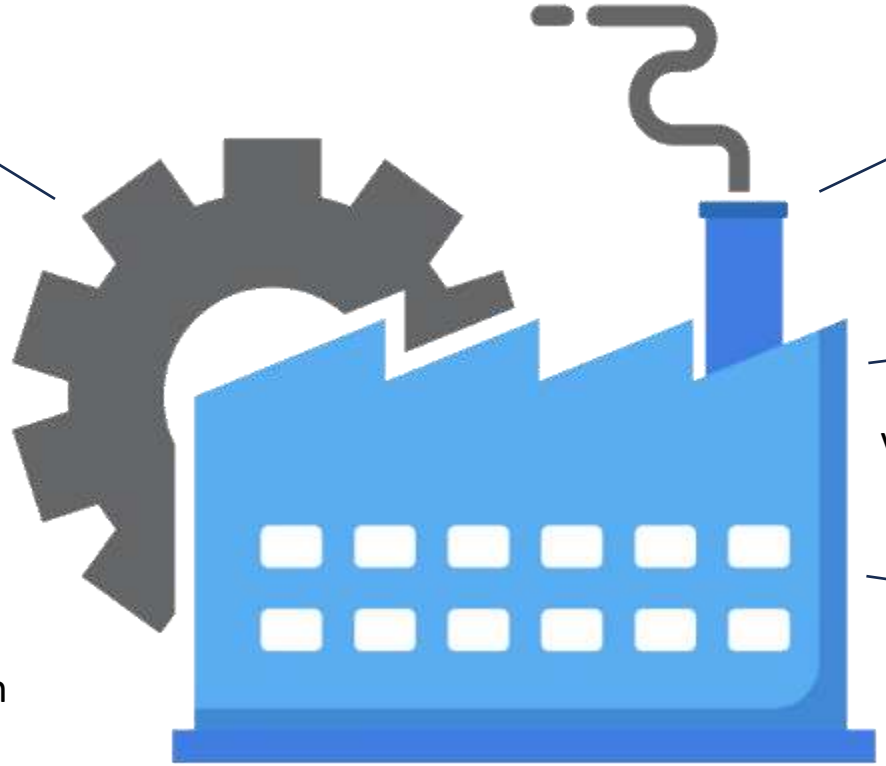
Real-time control, protocol adaptation, edge-computing

Predictive Maintenance

Real-time monitoring of equipment & health + analytics

Data Processing & Acceleration

Signal processing of computationally intensive tasks, compression & encryption



Industrial IoT Solutions

Hardware flexibility for changing requirements & security

Digital Twin Enhancement

Real-time capabilities to handle large volumes of data in closed-loop systems

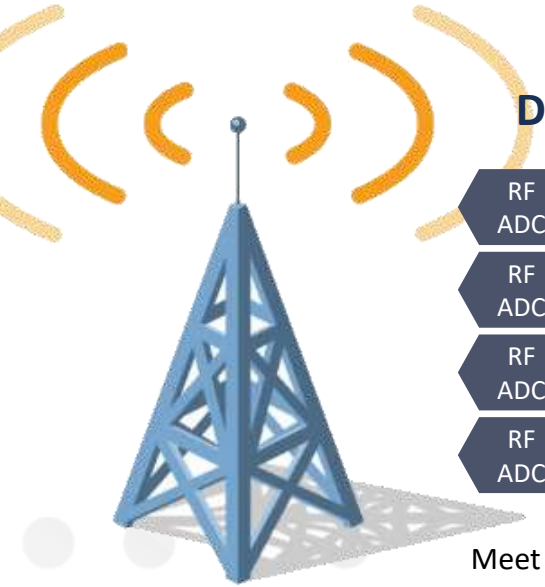
Embedded Vision

Sensor fusion with acceleration of computer vision software

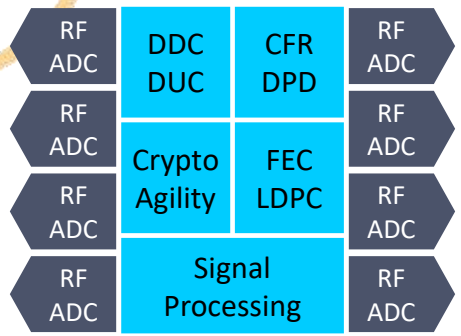
Robotics *Motor Control* *Gateways* *Additive MFG* *PLCs* *Smart Grid* *Machine Vision* *HMI* *Surveillance*

Comms Application Benefits from Adaptable Hardware

Software-Only Solutions Cannot Achieve Throughput and Latency Requirements

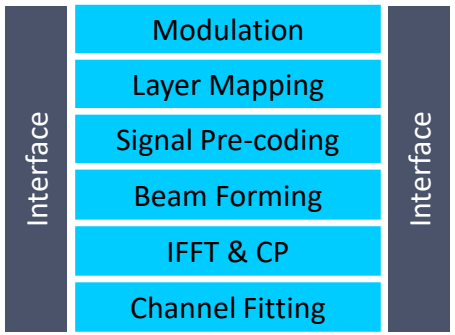


Digital Front End



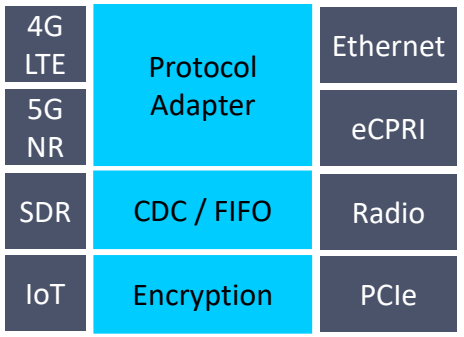
Meet Diverse & Advancing Radio Requirements
Optimized **eFPGA** supports demanding digital up & down conversion, predistortion, crest factor reduction, and signal processing

Spectral Efficiency



Massive MIMO requires scalability to meet size, weight, area & power requirements
High performance **eFPGA** enables users to optimize partitioning and integration of complex RF Signal Processing functions.

Multi Connectivity



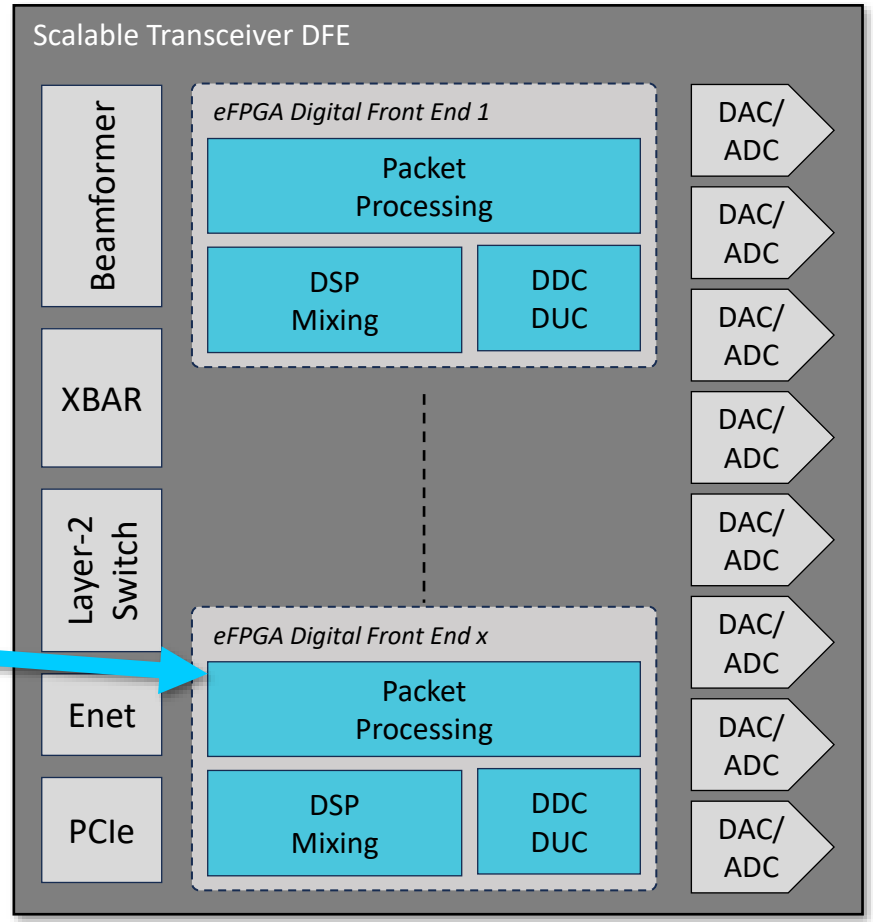
Converging disparate radio source to back haul networks requires adaptable protocol converters
Adaptable **eFPGA** provides the ability to bridge between a variety of radio and backhaul systems

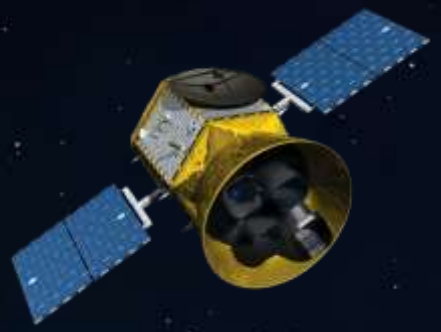
Baseband Unit

Scalable 5G Transceiver Digital Front End

- 5G performance and scalable solution
  - Adaptable to evolving 5G specifications
- Integrated system solution replacing traditional costly FPGAs
- Full speed FPGA performance at a fraction of the cost and power integrated in the SoC

Menta eFPGA IP manages packet processing, user logic and physical layer subsystems, & signal processing





menta

KEY ADVANTAGES OF MENTA EFPGA IN AEROSPACE & DEFENSE

Extend Mission Capabilities

Flexible, low-cost modernization with adaptable hardware

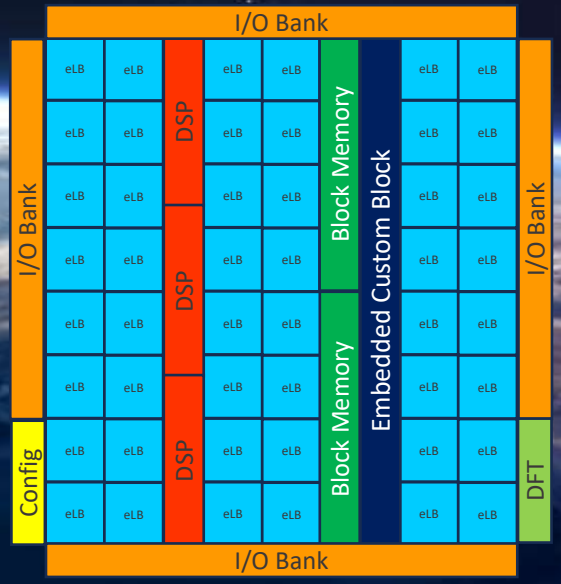
Algorithm Acceleration

Parallel & pipelined architecture for superior processing performance

Real-Time Data Processing

Isolated data & memory for deterministic processing

100% ADAPTABLE eFPGA ARCHITECTURE



Adaptable, Robust Security

Hardware accelerated cryptography agility & autonomy; IP Obfuscation

Foundry Rad-Hard Ready

Build with rad-hard cells to meet your harsh environment requirements

Radiation Tolerance

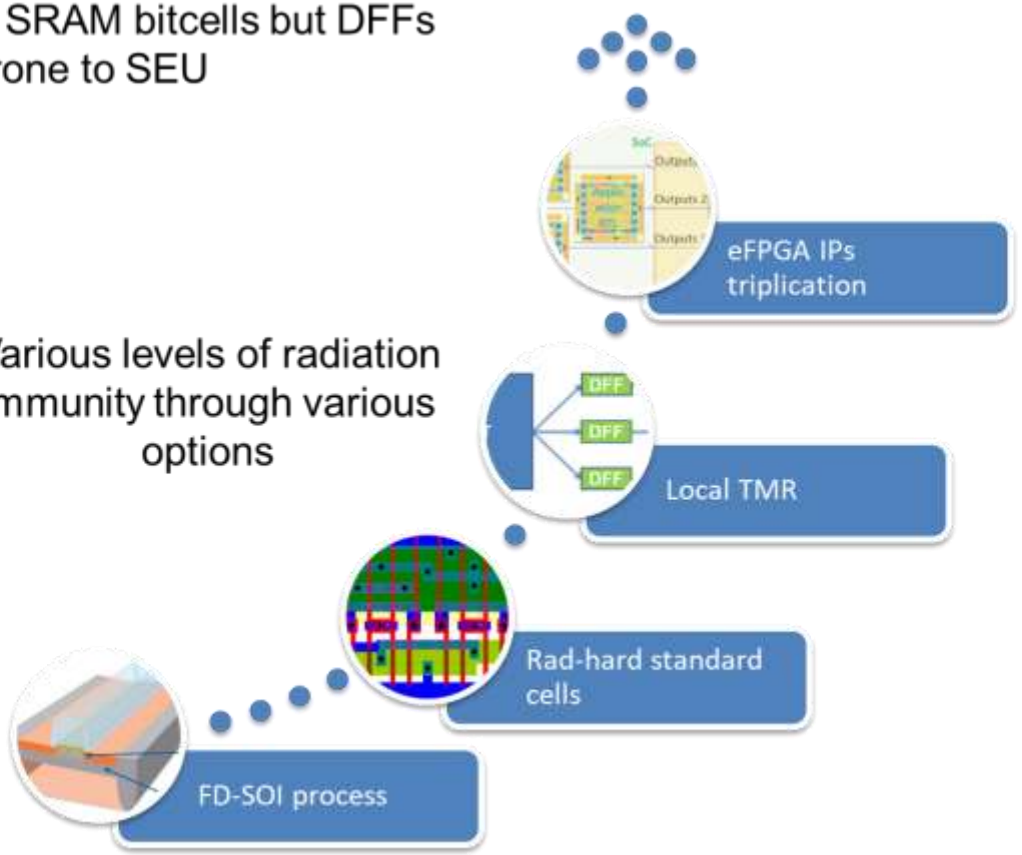
Menta's IP is 100% standard cell including configuration memory

Rad-Hard eFPGA IP - HowTo

Menta eFPGA IPs do not use SRAM bitcells but DFFs

- Naturally much less prone to SEU

Various levels of radiation immunity through various options



Rad-hard eFPGA IP in Mixed Signal IC

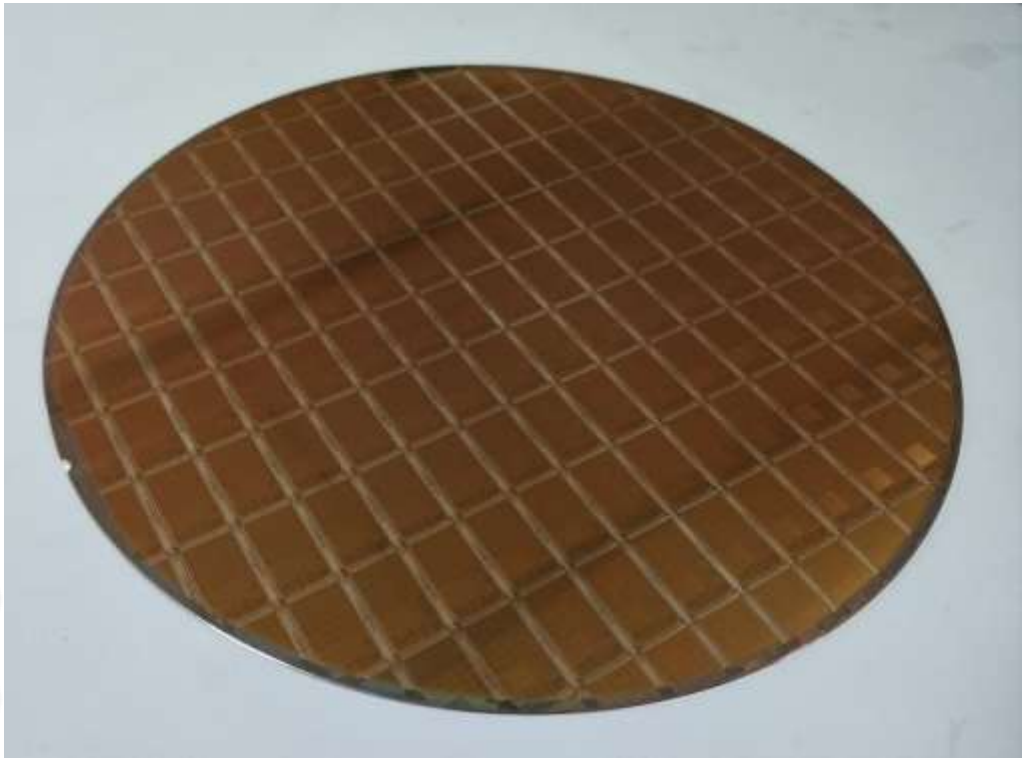
Accomplishing PROMISE, PROgrammable MIxed Signal ASIC Electronics Framework

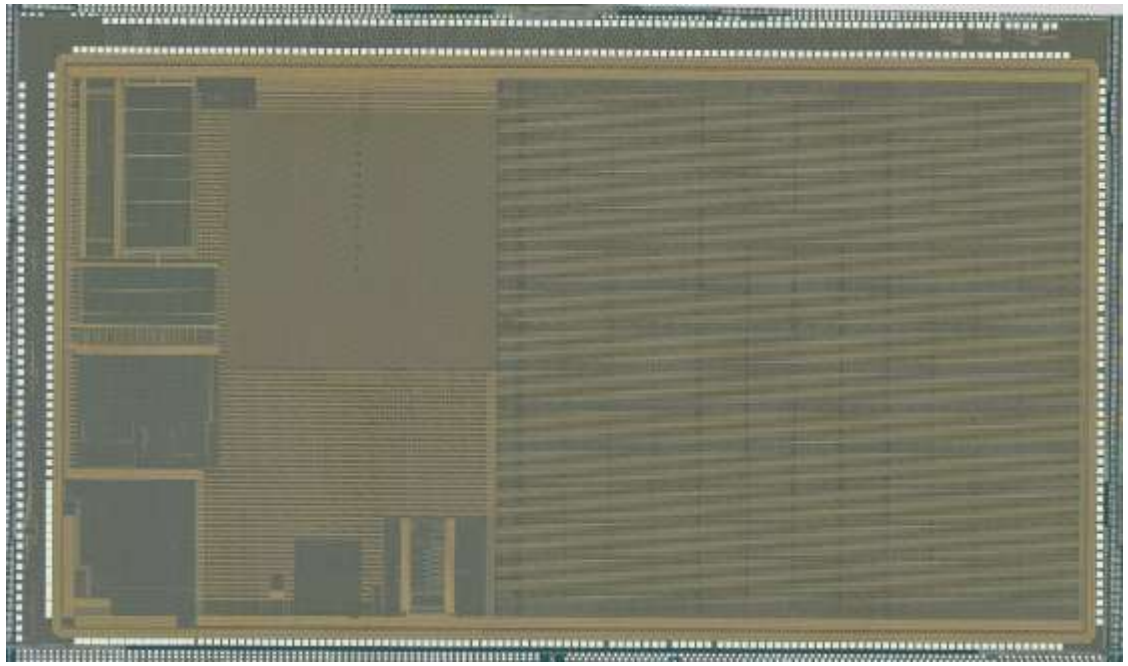
The PROMISE project objectives are to optimize the design cost, shorten schedule and de-risk analogue and mixed ASIC radhard design, manufacturing and qualification according to the needs of the space industry. PROMISE, led by Thales Alenia Space, encompasses diverse European partners, subcontractors, potential users and solution providers, all top actors of the European Mixed Signal ASIC ecosystem. The partners involved are: Thales Alenia Space in Spain (who leads the project), top level SMEs as ISD (Greece) and MENTA (France), key technological institutes such as IMEC (Belgium), IT (Portugal) and VTT (Finland); and a leading satellite manufacturer as Thales Alenia Space in France.

Fig. 2. PROMISE Pilot Circuit package

- XFAB 180 rad-hard
- eFPGA IP equivalent to Microsemi RTSX32SU FPGA
  - The reference for small rad-hard FPGA
  - Very expensive
  - Under severe export & ITAR control
- Applications: Remote Terminal Unit, Instrument Control Unit, RF Unit, Power controller, Motor control
- The eFPGA IP is running all digital algorithms
- Re-usable IP for all European Space projects

Rad-hard eFPGA IP in Mixed Signal IC





Embedded FPGA Applications & Benefits in Chiplets

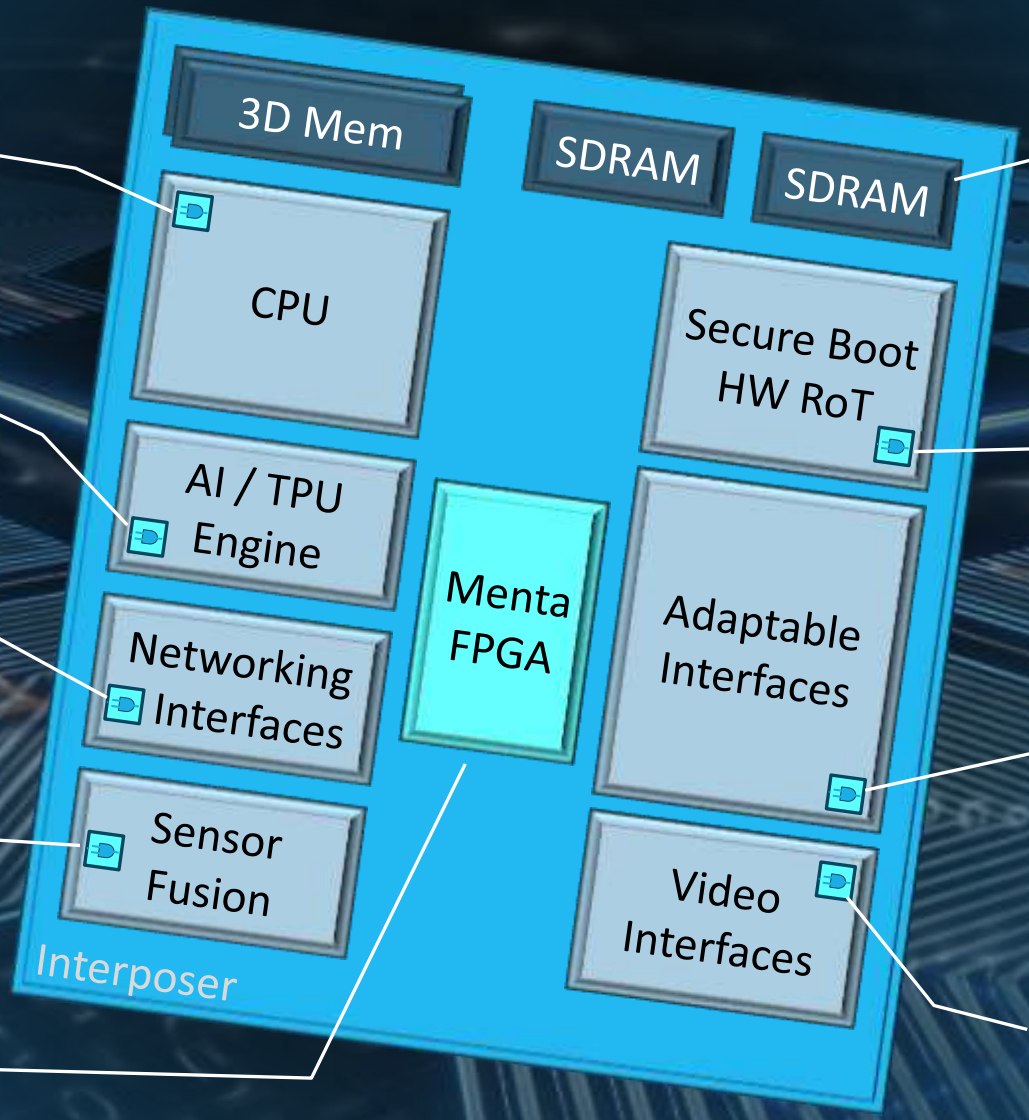
SW Acceleration with Custom Instructions & co-processing

Support for varying data paths & novel AI algorithms

Packet Processing & Transport Layer Security

Flexible & deterministic data pre-processing

Interposer Interface mapping & obfuscation Protocol Bridging (AXI, CHI)



Memory Masking, Mapping & Encryption

Crypto Agility
Security Autonomy
Obfuscation
Adaptive Side-channel Attack & Anti-Tamper

Protocol Adaptation
Data Buffering
Clock Synchronization

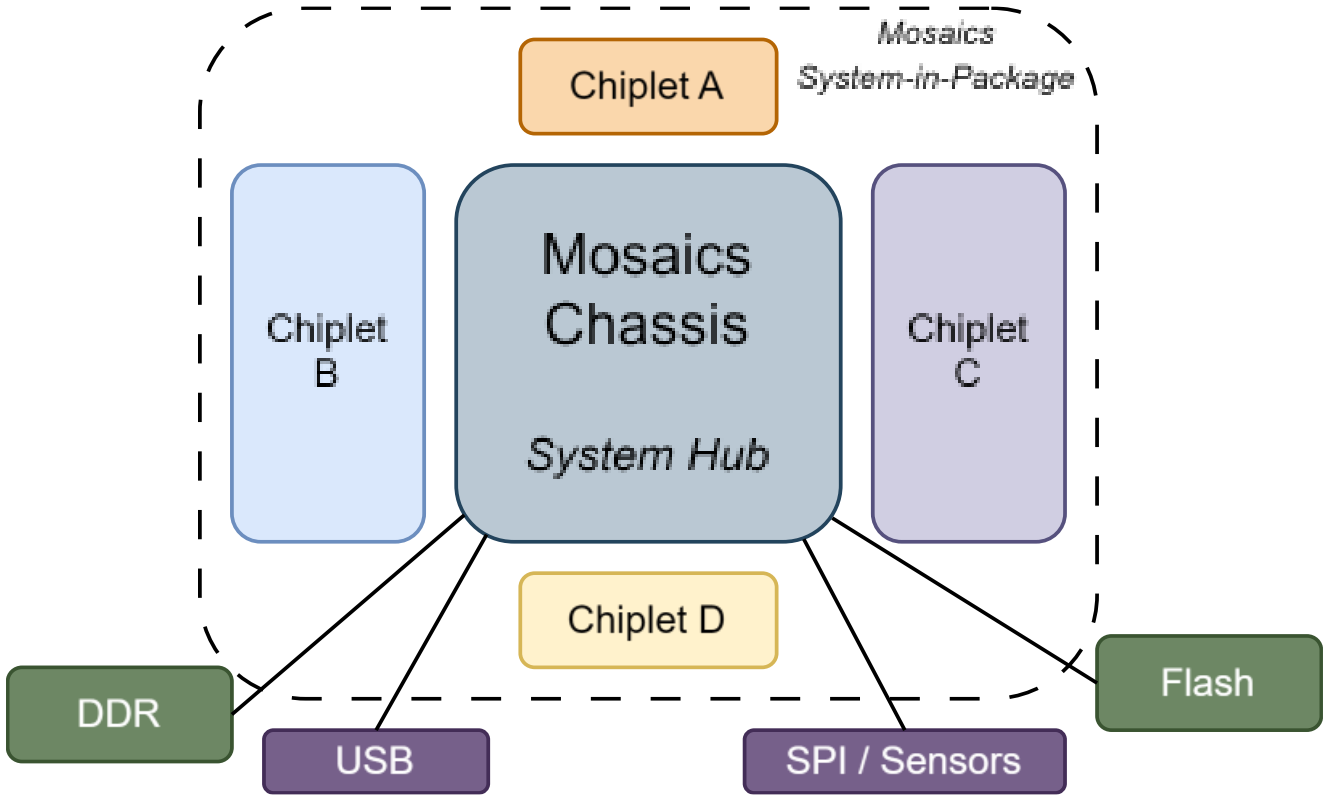
Adaptable Image Signal Processing for different protocols, encoding, resolution & frame rates

MOSAICS – SiP Development Platform

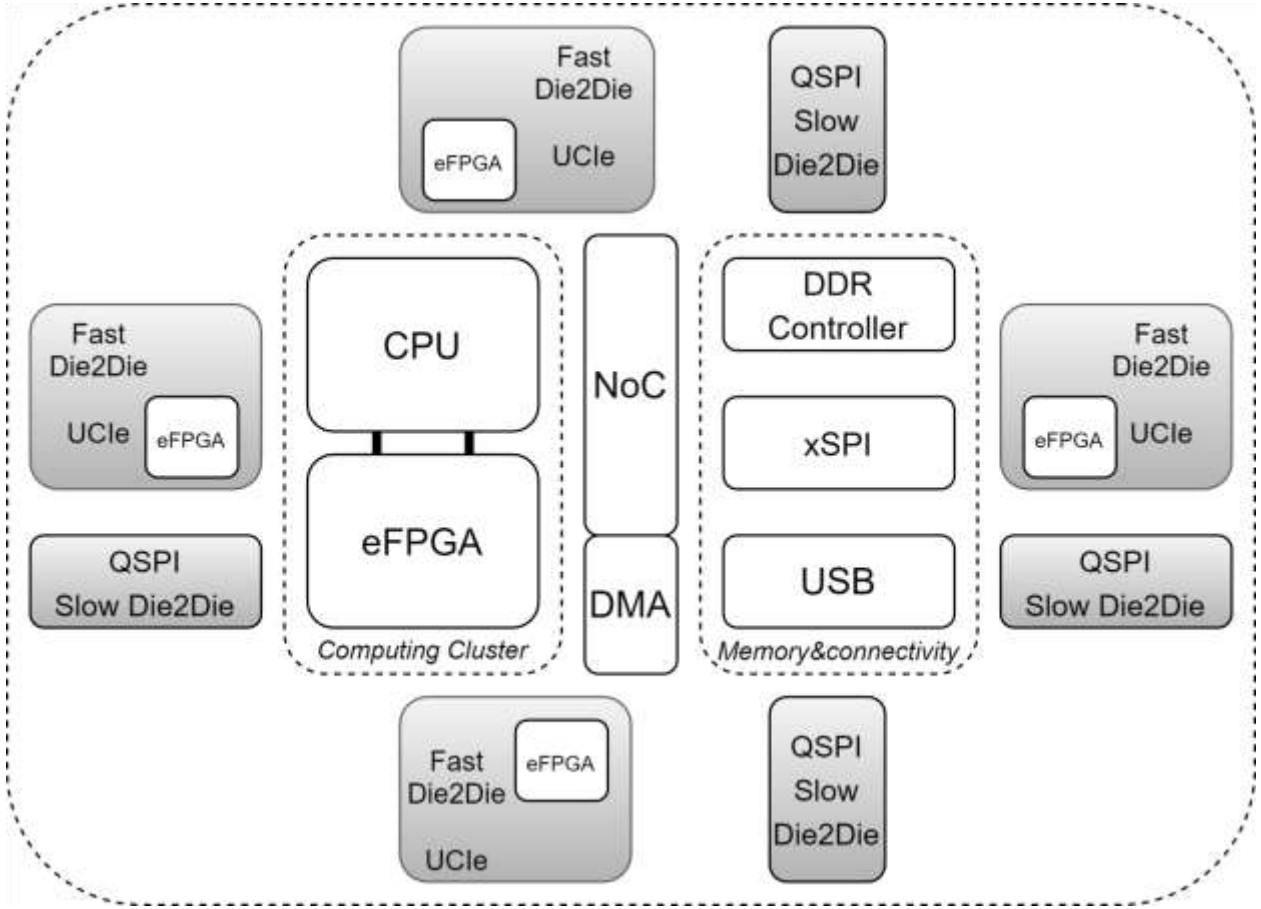
The Mosaics Platform enables heterogeneous SiP development using the Mosaics Hub and third-party chiplet catalog.

10x less System NRE

4x Faster TTM

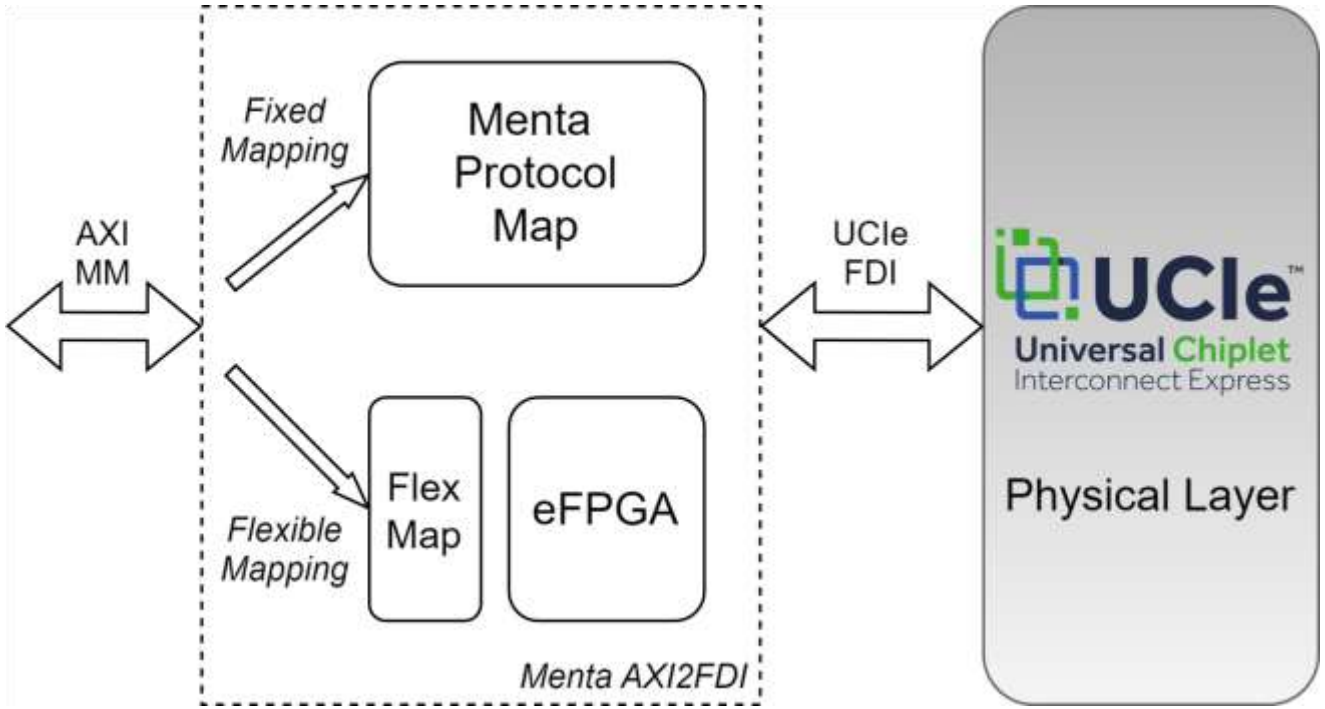


MOSAICS Chassis™



UCIe interoperability

Future-proof your chiplet infrastructure investment



Menta: the Clear Choice for Embedded FPGA

Performance, Control, Speed, and Support – in one IP.

Lowest Overall Cost

- Small die area
- Competitive licensing & royalty fees
- Highly efficient standard cell scan test (99.8%)
- Projected highest yield with 100% standard cell flow (no custom)

Fastest Time To Market

- IP (RTL + SW) delivery in less than 2 weeks
- Rapid ECO at any time
- Lowest risk - Foundry sign-off standard cells & flow
- Adaptability to any standards (automotive, industrial, defense)

Superior Support

- High-level of dedication
- Quick support turnaround
- Full IP and EDA ownership
- Global technical resources

Full Architectural Control

- Unlimited HW & SW definition / flexibility, hard macro
- Full control of physical implementation
- No reliance on 3rd-party tools - access, NRE/licensing cost

Full EDA Ownership & Customization

- 100% Integrable
- Easily Redistributable

Dedicated IP Partner

- Focused on IP and EDA solution
- No product or competitive conflict
- Planned R&D & support expansion

menta
Unlimited Power
of Technology

Thank you!

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